REMARKS

Claims 1-24 are pending in this application. Claims 10, 11 and 23 are allowed. Applicants submit that no new matter has been added to the application.

Rejection - 35 U.S.C. § 102

The Examiner rejected claims 1, 2, 4, 5, 9, 12, 13, 15, 16, 20, 21, 22 and 24 under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent No. 4,623,996 (McMillen) Applicants respectfully traverse the rejection.

The invention of McMillen is directed to a packet switching node 20. As described at Fig. 1 and col. 5, lines 35-47, the packet switching node 20 comprises N input ports 21 which are individually coupled to inputs of N queue selectors 22. Each of the queue selectors 22 has M outputs which are individually coupled to separate queues of a corresponding queue set 23 of size MXN. M output ports 25 are individually coupled to outputs of M output arbitrators 24. Each of the output arbitrators 24 has N inputs which are coupled to predetermined outputs of queues contained in each of the queue sets 23

As further described at col. 8, line 12 to col. 9 line 56 and Fig. 13, McMillen switches each incoming packet through the switch using a three phase clock which generates REQΦ, GRAΦ and XFERΦ signals. Initially, a tag decoder 40 decodes the tag bits of a packet input to one of the queue selectors based on the REQ signal (col. 8, lines 36-46), and selects one of the queues connected to the queue selector. If the queue connected to the queue selector is not full, the input packet is transferred to the queue based on the XFER signal (col. 8, lines 65-67). A status counter signals the arbitrator 24 when the queue is not empty which then requests to output a packet from the front of the queue to the corresponding output port (col. 9, lines 18-21). Referring now to Fig. 13, it can be seen by comparing the trailing edge of the FRONT signal to the REQ signal that the transfer of a packet from the input of a queue selector to the output of an arbitrator requires at least two cycles of the REQ and XFER signals.

The present invention comprises an input module 112 having M inputs and B outputs, a packet buffer 106 comprising B registers and an output module 114 having B inputs and N outputs. The present invention further includes control logic which processes the header

information of each input packet in a parallel path to the payload information. The control logic consists of header hopper 132 which receives the header of each input packet and pre-assigned register addresses of available registers from a register selector 134, the register selector 134 which determines the status of each register, and queues 138 which manages the priority of conflicting packets based on the QoS of the input packets. A significant difference between the registers of the present invention and the queue set disclosed by McMillen is that no queues are formed in the individual registers of the present invention, thus facilitating a faster transfer between the input modules and the output modules than can be provided by McMillen's invention.

As further described at pages 12 – 13, the present invention switches input packets to the designated output port arriving in each in each of a sequence of time frames by pipelining the input packets through the input switch and a preassigned register to the designated output port within the time frame of the input packet. The pipe lining is accomplished by register selector 134, which determines the availability of a register 106 during the frame period prior to the frame of the incoming packet (current frame). Upon arrival of the of the packet at an input port of the input module in the current frame, the input module 112 switches the packet to the selected register 106. At some point in the current frame, and possibly before the packet has wholly entered the selected register 106, the output module 114 is set up by the register selector 134 and the contents of the register 106 is pipelined to the output port. Consequently, the packet is transferred from the input to the output port within the current time frame.

Claims 1, 2, 4, 5, 9, 12, 13, 15, 16, 20, 21, 22 and 24

Claim 1, representative of independent claims 12, 21 reads as follows:

An M×N packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports, the switch comprising

an input module, having M inputs and B outputs, B > M, for switching the M input packets to M of the B outputs to produce M switched packets during each of the frame times,

a packet buffer including B registers, coupled to the input module, for storing the M switched packets into M available registers during each of the frame times to produce M stored packets, and

> *an output module, having B inputs and N outputs coupled to the packet buffer, for transferring up to N packets from occupied registers in each of the frame times to the output ports based upon destination addresses contained within each of the stored packets.*

The Examiner states that McMillen discloses a packet switch that includes an input module that produces M switched packets during each of the frame times, a packet buffer that stores the M switched packets during each of the frame times and an output module that transfers N of the M switched packets from the registers in each of the frame times. Applicants respectfully disagree.

As discussed above, the packet switch disclosed by McMillen requires at least two frame times to move a packet from the input of the queues selector to the output of the arbitrator. In contrast, claims 1, 12, 21 and 24 recite transferring M input packets from the M inputs of the input module to M outputs in each of the frame times, storing M packets to the registers in each of the frame times and transferring N packets from the registers to the N outputs of the output module in each of the frame times. Applicants submit that McMillen does not disclose all the elements of claims 1, 12, 21 and 24. Accordingly, Applicants respectfully request reconsideration and withdrawal of the 102 rejection of claims 1, 12, 21 and 24.

With respect to claims 2 and 13, the Examiner states that the input modules and the output modules disclosed by McMillen are crossbar switches. Applicants respectfully disagree.

A crossbar switch is well known to be a switch which can connect any input path to any output path. (See IEEE 100, The Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, 2000, page 252.) In contrast, the input switch comprising N queue selectors, each of which having a single input port and the output switch comprising M arbitrators, each of which having only a single output port may only select the queues in the queue set which are physically connected to the individual queue selector/arbitrator, and are unable to select any output/input from each of the input/output ports.

Further, it is respectfully submitted that since claims 1, 12, 21 and 24 have been shown to be allowable, claims 2, 4-6, and 8-9, dependent on claim 1, claims 13, 15-17 and 19-20

dependent on claim 12 claim 22 dependent on claim 21 are allowable, at least by their dependency. Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the §102 rejection of claims 2, 4-5, 9, 13, 15-16 and 20.

Rejection - 35 U.S.C. § 103

The Examiner rejected claims 3, 4, 7 and 18 under 35 U.S.C. § 103 as being unpatentable over McMillen in view of U.S. Patent No. 5,583,861 (Holden). Applicants respectfully traverse the rejection.

Holden is directed to an ATM switching system comprising a switch fabric (Fig. 2) of a plurality of switch element circuits (Figs. 3 and 5) and routing table circuits (Abstract). Each switch element circuit includes a shared cell buffer pool (col. 2, lines 56-57). All cells passing though one of the switch elements are written into an associated cell buffer pool during a first cell cycle and connected to the switch element output at a later cell cycle.

Claims 3 and 14

With respect to claims 3 and 14, the Examiner states that McMillen does not disclose a one-stop shared buffer memory, but that Holden discloses such a memory and it would have been obvious to a person skilled in the art at the time of the invention to modify McMillen to use the one stop shared buffer memory taught by Holden. Applicants respectfully traverse the rejection.

Claims 3 and 14, dependent on claims 1 and 12 respectively, recite, *inter alia*, a packet switch comprising a one-stop shared buffer memory. As defined on page 3 of the application, a one-stop buffer in the context of a packet switch, is a type of packet buffer in which a packet stored in the buffer occupies a single register in the buffer from its initial storage in the buffer until its eventual exit from the packet switch.

Holden does not disclose, teach or suggest a one-stop buffer memory. The cell (packet) buffer pools disclosed by Holden are associated with each element of the switch fabric. As such, a packet is written and read from each cell buffer pool as the packet makes its way from one switch element to the next switch element as the packet transits through the switch fabric. Thus, a packet does not remain in a single memory location over the entire time that the packet is

transitioning through the switch and therefore the shared memory pool disclosed by Holden can not be characterized as a one-stop buffer.

Neither McMillen nor Holden disclose, teach or suggest a one-stop shared buffer memory as recited in claims 3 and 14. Further, Holden does not teach or suggest a packet switch which switches M input packets to N output ports in each of a sequence of frame times as recited in claims 1 and 12. Consequently, Holden does not make up for the deficiency of McMillen. Accordingly, Applicants respectfully request reconsideration and withdrawal of the §103 rejection of claims 3 and 14.

Claims 7 and 18

The Examiner states that McMillen discloses N queues for storing the addresses of the assigned registers in each of the frame times based on destination information in the packet header but does not receive the address information from the header hoppers. The Examiner further states that Holden discloses a header register set as header hoppers and it would have been obvious to one of ordinary skill in the art at the time of the invention to use header hoppers such as taught by Holden.

Applicants respectfully submit that the Examiner has misconstrued Fig. 6 and the discussion at col. 6, lines 49-56. As described at col. 6, lines 49-56, Holden uses a linked list to maintain first-in/first-out queues by means of pointers to the next entry in the cell memory. For each of the queues, a buffer pointer is constructed from the head address and from the tail address of the queue and stored in the head register set 153 and the tail register set 155. Thus, as made clear by Holden, the head register set 153 does not store header information as asserted by the Examiner. Consequently, Holden can not possibly teach or suggest transmitting the addresses of assigned registers from a header hopper to the N queues based on destination information in the header information, as recited in claims 7 and 18.

Further, Holden does not teach or suggest a packet switch which switches M input packets to N output ports in each of a sequence of frame times as recited in claims 1 and 12. Consequently, Holden does not make up for the deficiency of McMillen. Accordingly,

Applicants respectfully request reconsideration and withdrawal of the §103 rejection of claims 7 and 18 dependent on claims 1 and 12 respectively.

Allowable Subject Matter.

Claims 6 and 8 depend from allowable claim 1 and claims 17 and 19 depend from allowable claim 12. Accordingly claims 6, 8, 17 and 19 are allowable, at least by their dependency. Accordingly, Applicants respectfully request reconsideration and withdrawal of the objection to claims 6, 8, 17 and 19.

Conclusion

Insofar as the Examiner's rejection has been fully addressed, the instant application is in condition for allowance. Issuance of a Notice of Allowability of all pending claims is therefore earnestly solicited.

Respectfully submitted,
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